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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,554	01/30/2002	Douglas Hooker Bradley	AUS920010743US1	5802

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EXAMINER	
DO, CHAT C	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/059,554	BRADLEY ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 October 2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2,3,8,9,12,13,15,16,18,19 and 21-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2,3,8,9,12,13,15,16,18,19 and 21 is/are rejected.

7)☒ Claim(s) 22-25 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 10/22/2006.

2. Claims 2-3, 8-9, 12-13, 15-16, 18-19, and 21-25 are pending in this application. Claims 3 and 13 are independent claims. In Amendment, claims 1, 4-7, 10-11, 14, 17, and 20 are cancelled and claims 21-25 are added. This Office Action is made final.

Claim Objections

3. Claims 3 and 13 are objected to because of the following informalities:

Re claim 3, the applicant is advised to write the acronym "CMOS" in full for clarification. Claim 13 has the same objection.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 2-3, 8-9, 12-13, 15-16, 18-19, and 21 are rejected under 35 U.S.C. 102(a) as being anticipated by Hayakawa (U.S. Patent No. 2001/0037349).

Re claim 2, Hayakawa further discloses in Figures 21 each generate bit is the logical AND of its corresponding bits in the first and second operand (Figure 21(c)), each propagate bit is the EXOR of its corresponding bits in the first and second operands (Figure 21(a)), and each kill bits is the logical NOR of its corresponding bits in the first and second operands (Figure 21(b)).

Re claim 3, Hayakawa discloses in Figure 19 an adder circuit for determining the sum of two operands (e.g. left column page 1 paragraph 0008), comprising: a set of PGK (Figure 19 to product K0-K31, P0-G31, and G0-G31 prior entering Stage-0) circuits configured to generate propagate (P), generate (G), and kill (K) bits corresponding to at least a portion of the first and second operands (e.g. a and b operands in left column page 1 paragraph 0008); at least one tier of group circuits (e.g. Stage-0 in Figure 19) configured to receive the propagate, generate, and kill bits from a plurality of the PGK circuits and to produce, in response thereto, a set of group propagate, generate, and kill values (output of all 4-bit CLA); a carry generation circuit (Stage-2) configured to receive a carry-in bit (e.g. Cin and bar(Cin) in Stage-2) and the outputs of at least one of the group circuits (e.g. PGGG/GGG/KGGG) and further configured to generate a carry-out bit (C<31> in Stage-2) representing the carry-out of the corresponding group; and a select circuit (e.g. left column page 1 paragraph 0008) configured to select between a first sum and a second sum responsive to the carry-out bit; wherein at least one of the PGK circuits, group circuits, and carry circuits includes at least one CMOS transmission gate (e.g. any Figure in Figures 21 and paragraph [0086]).

Re claim 8, Hayakawa further discloses in Figure 19 the at least one tier of group circuits (e.g. Stage-0; Stage-1; Stage-2) includes a first tier of group circuits configured to receive the output of the PGK circuits and to generate an intermediate set of group propagate, generate, and kill values (e.g. Stage-1) and a second tier (e.g. Stage-2) of at least one group circuit configured to receive the intermediate set of group propagate, generate, and kill values and to produce a final group propagate, generate, and kill values.

Re claim 9, Hayakawa further discloses in Figure 19 the intermediate group of propagate, generate, and kill values (e.g. PGG, GGG< KGG) each corresponds to a group of four adjacent bits and further wherein the final group of propagate, generate, and kill values correspond to a group of 16 adjacent bits (e.g. first 4-bit CLA corresponding to first 16 bits).

Re claim 12, it is a microprocessor claim of claim 2. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 13, it is a microprocessor claim of claim 3. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 15, Hayakawa further discloses in Figures 19 and 21 the PGK circuits farther generate the logical complements of the propagate, generate, and kill bits substantially simultaneously with the generation of the propagate, generate, and kill bits (Figures 19 and 21(a)-21(c)).

Re claim 16, Hayakawa further discloses in Figure 19 the group circuits further generate the logical complements of the group propagate, generate, and kill values (e.g. 0147 in page 9).

Re claim 18, it is a microprocessor claim of claim 8. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 19, it is a microprocessor claim of claim 9. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 21, Hayakawa further discloses in Figures 19 and 21 the CMOS transmission circuit comprises a PMOS transistor and an NMOS transistor, wherein a first source/drain terminal of the PMOS transistor is connected to a first source/drain terminal of the NMOS transistor and wherein a second source/drain terminal of the PMOS transistor is connected to a second source/drain terminal of the NMOS transistor (e.g. Figure 9).

Allowable Subject Matter

6. Claims 22-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

7. The amendment filed 10/22/2006 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

The changes in Figure 7 would introduce new matter into the disclosure. The applicant is requested to point out clearly the support of changes in the original disclosure.

Applicant is required to cancel the new matter in the reply to this Office Action.

Response to Arguments

8. Applicant's arguments filed 10/22/2006 have been fully considered but they are not persuasive.

a. The applicant argues in pages 16-17 for claims that the cited reference by Hayakawa fails to disclose the use of CMOS transmission gate as defined in the specification as a PMOS and NMOS transistor combination in which a first source/drain of the PMOS transistor is connected to a first source/drain terminal of the NMOS transistor and a second source/drain terminal of the PMOS transistor is connected to a second source/drain terminal of the NMOS transistor as cited in the claim.

The examiner respectfully submits that the independent claims 3 and 13 do not clearly define or address how the CMOS transmission gate is structured. The cited reference clearly defines several places that CMOS transmission technology is used as composed of PMOS and NMOST for form logic circuits for determining the PKG. Further, Figures 6-9 disclose logic circuits using the PMOS (e.g. Figure 6 PC3) and NMOS (e.g. Figure 6 N33) gates with structure as defined as a first source/drain of the PMOS transistor is connected to a first source/drain terminal of the NMOS transistor (e.g. a PC3 with N33 in Figure 6) and a second source/drain terminal of the PMOS transistor is

connected to a second source/drain terminal of the NMOS transistor (e.g. PC1 and N11 in Figure 6).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

April 6, 2007

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